Abstract

The present invention relates to the design of highly reliable high performance microprocessors, and more specifically to designs that use cache memory protection schemes such as, for example, a 1-hot plus valid bit scheme and a 2-hot vector cache scheme. These protection schemes protect the 1-hot vectors used in the tag array in the cache and are designed to provide hardware savings, operate at higher speeds and be simple to implement. In accordance with an embodiment of the present invention, a tag array memory including an input conversion circuit to receive a 1-hot vector and to convert the 1-hot vector to a 2-hot vector. The tag array memory also including a memory array coupled to the input conversion circuit, the memory array to store the 2-hot vector; and an output conversion circuit coupled to the memory array, the output conversion circuit to receive the 2-hot vector and to convert the 2-hot vector back to the 1-hot vector.